WHAT IS CLAIMED IS:

1. A transistor with π -gate structure, with a GaAs wafer formed on the bottom with GND, which is grounded to source layers formed on the top surface of the GaAs wafer by the process of back side via-hole, with a drain formed between the source layers, the top part of which has an air layer, and with a gate shaped, as the result of using the air bridge technique, such that it contacts the top surface of the GaAs wafer between the source layers and the drain and so supports both sides of the wafer over the air layer of the drain, whereby a gate having π -structure results.

2. A manufacturing method of gate with π -structure by using an air bridge technique comprises:

the step of vapor-depositing, on a wafer, to form a drain and source layers of Ti/Au as the primary metal layers in the thickness of 200 Å/4000 Å through PHEMT process;

the step of forming silicon nitride film in the thickness of 1000 Å, patterning the formed silicon nitride film by using an electron beam exposure device, forming gate foot steps by etching the film, and then conducting HMDS coating by PR-via pattern forming process using the positive photo irradiation drawing process, conducting AZ1518 coating at 2000 rpm for 20 seconds, conducting soft-baking at 98℃ for 45 seconds, aligning patterns, conducting UV exposure and developing for 1 minute and 30 seconds, and subsequently conducting a hard-baking at 115℃ for 4 minutes and 30 seconds to thereby harden the resist;

the step of forming, by vapor-depositing, a thin gold film in the thickness of about 250~300 Å on the surface of GaAs wafer;

the step of conducting HMDS coating after forming secondary metal patterns by using an image inversion process, conducting AZ5214E coating at 2000 rpm for 10 seconds, conducting soft-baking at 98℃ for 45 seconds, aligning patterns, and then conducting free exposure for 7 seconds, reverse baking at 110℃ for 50 seconds and

plot exposure for 25 seconds before development;

the step of disconnecting the source and drain by etching off the exposed gold film by using the metal etching solution consisting of N, KCN, H2O at the volume ratio of 10 : 500 : 100, and thereafter forming a gate in the thickness of 200Å/8000Å by vapor deposition of Ti/Au and attaining a finished gate with π -structure through lifting-off by means of acetone; and

the step of performing the process of back side via-hole on the wafer to ground the GND to the source layer.